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DC-link Capacitor Voltage Regulation with Effort-reduction Fuzzy Logic Control for Three-level Inverter-based Shunt Active Power Filter

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ABSTRACT

Shunt active power filter (SAPF) is the most effective solution for current harmonics. In its controller, DC-link capacitor voltage regulation algorithm with either proportional-integral (PI) or fuzzy logic control (FLC) technique has played a significant role in maintaining a constant DC voltage across all the DC-link capacitors. However, PI technique performs poorly with high overshoot and significant time delay under dynamic state conditions, as its parameters are difficult to be tuned without requiring complete knowledge of the designated system. Although FLC technique has been developed to overcome limitations of PI technique, it is mostly developed with high complexity thereby increases computational burden of the designed controller. This paper presents a fuzzy-based DC-link capacitor voltage regulation algorithm with reduced computational efforts to enhance performance of three-phase three-level neutral-point diode clamped (NPC) inverter-based SAPF in overall DC-link voltage regulation. The proposed method is called effort-reduction FLC technique. The proposed algorithm is developed and evaluated in MATLAB-Simulink. Moreover, conventional algorithm with PI technique is tested for comparison purposes. Simulation results have confirmed improvement achieved by the proposed algorithm in comparison to the conventional algorithm.

Keywords: Active power filter, current harmonics, DC-link voltage control, fuzzy logic control (FLC), multilevel inverter

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INTRODUCTION

High current harmonics resulting from intensive use of nonlinear loads such as power converters and adjustable speed drives is recognized as a major issue for a power system. The presence of current harmonics not only degrades overall system efficiency

by worsening its power factor (PF) performance, but it also causes other associated problems such as equipment overheating, failures of sensitive devices and capacitor blowing (Dai & Dai, 2008; Kale & Ozdemir, 2005a). It is compulsory to minimize the harmonics level of a power system. Shunt-typed active power filter (SAPF) is the most effective solution to current harmonics, where all the undesired current components are eliminated by injecting opposition current (simply known as injection current) back to the polluted power system. In addition, it also provides reactive power compensation meant for improving PF performances (Jain & Gupta, 2014; Kale & Ozdemir, 2005b).

Most of the established SAPFs employ a standard two-level inverter topology in their design. However, three-level inverters which have been reported to be more advantageous than traditional two-level inverters in term of output voltage quality and power losses are accepted as better alternatives (Hoon et al., 2016a, 2016b). The performance of SAPF in current harmonics mitigation is dependent on the performance of its controller. Specifically, its controller consists of harmonics extraction, DC-link capacitor voltage regulation and switching (current control) algorithms. The DC-link capacitor voltage regulation algorithm plays an important role in maintaining a constant overall DC-link voltage for a typical inverter-based SAPF. The DC-link voltage must be maintained at a level high enough to ensure successful generation of injection current. Moreover, in a three-level neutral-point diode clamped (NPC) inverter, voltage across the two splitting DC-link capacitors has to equally be maintained as half of the overall DC-link voltage so that a balanced injection current can be generated to properly mitigate the current harmonics.

The overall DC-link voltage is often regulated by manipulating the voltage error resulting from the difference between the actual overall DC-Link voltage and its reference voltage counterpart to estimate an output, which is assumed to be the main control signal for regulating DC-link voltage. Traditionally, the voltage error manipulation and control signal estimation processes are done with a proportional-integral (PI) controller (Afghoul & Krim, 2012; Jain et al., 2002; Karuppanan & Mahapatra, 2010, 2012; Suresh et al., 2012) due to its simple implementation features. However, it performs poorly with large overshoot (Afghoul & Krim, 2012; Jain et al., 2002; Suresh et al., 2012) and serious time delay (Afghoul & Krim, 2012; Jain et al., 2002; Karuppanan & Mahapatra, 2010, 2012) under dynamic state conditions. Moreover, the performance of PI controller is strictly dependent on its tuned proportional gain and integral gain parameters which are normally obtained through a tedious heuristic approach. Besides, the tuning process can be difficult as SAPF does not possess a precise linear mathematical model which is needed to accurately tune the gain parameters of PI controller (Jain et al., 2002; Karuppanan & Mahapatra, 2012).

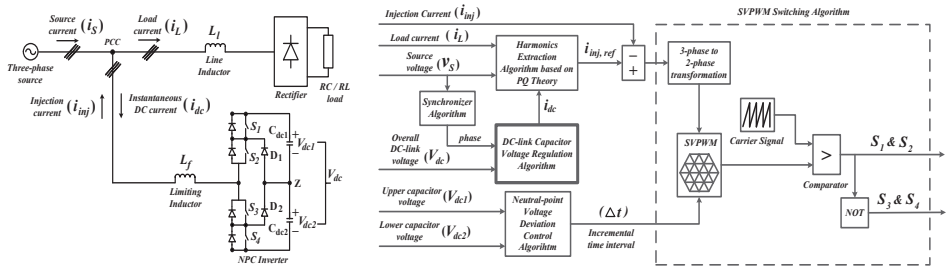
Further improvement based on artificial intelligence (AI) technique using fuzzy logic controller (FLC) is employed to overcome limitations of PI controller. By incorporating advantages of FLCs the performance of SAPF in DC-link voltage regulation was significantly improved (Afghoul & Krim, 2012; Jain et al., 2002; Karuppanan & Mahapatra, 2010, 2012). Basically, FLC is an adaptive mechanism which is capable of approximating a function based on simple linguistic control (if-then) rules (Belaidi et al., 2012; Suresh et al., 2012;

Zainuri et al., 2016). As a result, it is able to work effectively with imprecise inputs, handle nonlinear system with parameter variations, and is possible to be designed without knowing the exact mathematical model of the system (Belaidi et al., 2012; Karuppanan & Mahapatra, 2010, 2012; Mikkili & Panda, 2012; Zainuri et al., 2016). However, the FLC technique that is used is implemented with high complexity: 7×7 fuzzy membership functions (MFs) with 49 control rules (Afghoul & Krim, 2012; Belaidi et al., 2012; Jain et al., 2002; Karuppanan & Mahapatra, 2010, 2012; Mikkili & Panda, 2012; Suresh et al., 2012), and imposes great computational burden to the controller. Lower numbers of fuzzy MFs and control rules have never been considered as they are reported to be incapable of maintaining the overall DC-link voltage constant (Mikkili & Panda, 2012).

This paper presents a DC-link capacitor voltage regulation algorithm with effort-reduction FLC technique to efficiently control the overall DC-link voltage of three-phase three-level NPC inverter-based SAPF. The proposed effort-reduction FLC technique is developed by considering a reduced amount of fuzzy MFs and control rules, thereby reducing both design efforts and computational burden of the designed controller. The design concept and effectiveness of the proposed algorithm are verified using MATLAB-Simulink. The paper is organized as follows. In Section 2, the proposed SAPF with control strategies is described. Section 3 provides detailed descriptions on the proposed algorithm. The simulation findings are presented, and discussed in Section 4 showing improvements achieved by the proposed algorithm in comparison to the conventional algorithm. A brief summary is provided at the end of the paper, highlighting significant contributions of this work.

SHUNT ACTIVE POWER FILTER (SAPF) WITH CONTROL STRATEGIES

The proposed three-phase three-level NPC inverter-based SAPF system and its control strategies are shown in Figure 1. The control strategies compose of harmonics extraction, DC-link capacitor voltage regulation, synchronizer, neutral-point voltage deviation control, and switching control algorithms.



(a) (b)

Figure 1. The proposed three-phase three-level NPC inverter-based SAPF: (a) circuit diagram, and (b) control strategies

The main focus of this paper is on the DC-link capacitor voltage regulation algorithm. From the literature, in order to ensure proper generation of injection current i_{injs}, the overall DC-link voltage V_{dc} is set according to the following requirement (Khadem et al., 2014)

$$v_s < v_{SAPF\_max} \leq 2v_s \tag{1}$$

$$V_{dc} = 2v_{SAPF\_max} \tag{2}$$

where v_s represents the source voltage, and v_{SAPF_max} represents the maximum output voltage of SAPF.

The minimum capacitance value C_{dc} for each capacitor can be calculated as follows (Yao & Green, 2005)

$$C_{dc} \geq \frac{\left|\int_0^t i_{inj} dt\right|}{4\Delta V_{max}} \tag{3}$$

where i_{inj} represents the injection current, and ΔV_{max} represents the maximum voltage ripple allowed on DC-link capacitors.

For the purpose of the harmonics extraction algorithm, instantaneous power (PQ) theory (Belaidi et al., 2012; Hoon et al., 2016b) is used. Meanwhile, a synchronizer is employed to provide referencing signal to the DC-link capacitor voltage regulation algorithm. Furthermore, voltage balancing of splitting DC-link capacitors is achieved via neutral-point voltage deviation control algorithm (Bhalodi & Agarwal, 2010). Finally, the switching control is accomplished through 25 kHz Space Vector PWM (SVPWM) switching algorithm (Bhalodi & Agarwal, 2010).

PROPOSED DC-LINK CAPACITOR VOLTAGE REGULATION ALGORITHM

Below details of the conventional algorithm utilizing the PI technique is presented. This is followed with a presentation of the proposed algorithm with effort-reduction FLC technique.

Conventional DC-Link Capacitor Voltage Regulation Algorithm with PI Technique

Generally, the overall DC-link voltage is regulated by controlling the real power drawn by SAPF throughout its switching operation. The voltage regulation process is considered to have accomplished when the real power drawn by the SAPF is made equal to its switching losses. To ensure proper function of SAPF the magnitude of the generated reference current must be adjusted by manipulating the variable known as instantaneous DC current i_{dc} (refer to Figure 1). which is generated based on the difference between overall DC-link voltage and its desired reference voltage counterpart, so that a precise amount of real power can be drawn by SAPF, to compensate its potential losses.

As mentioned in Section 1, PI technique is the most widely utilized technique in the area of DC-link capacitor voltage regulation. Based on this technique, the voltage error resulting from the difference between overall DC-link voltage V_{dc} ($V_{dc1} + V_{dc2}$) and its reference voltage

$V_{dc1,ref}$ is directly manipulated by a PI controller to approximate the required amplitude I_{dc} of control signal i_{dc}. The control approach can be summarized as (5). The control signal i_{dc} is made available by multiplying I_{dc} with the reference angle delivered by a synchronizer.

$$E(k) = V_{dc,ref}(k) - (V_{dc1}(k) + V_{dc2}(k)) \tag{4}$$

$$I_{dc} = E\,(K_p + K_i \int dk) \tag{5}$$

Figure 2 shows the control structure of conventional DC-link capacitor voltage regulation algorithm with PI technique. Meanwhile, the minimum value of the design parameters used in the PI technique can be obtained as follows (Hoon et al., 2016a; Zainuri et al., 2016)

$$K_p \geq C_{dc}\xi\omega \tag{6}$$

$$K_i \geq C_{dc}\omega/2 \tag{7}$$

where K_p is the proportional gain, K_i is the integrator gain, C_{dc} is the capacitance value of each splitting capacitor, ξ is the damping factor fixed at 0.707, and ω is the angular frequency.

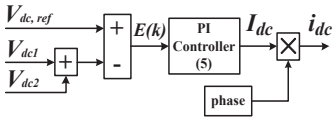


Figure 2. Control structure of conventional DC-link capacitor voltage regulation algorithm with PI technique

Proposed DC-Link Capacitor Voltage Regulation Algorithm with Effort-Reduction FLC Technique

The control structure of DC-link capacitor voltage regulation algorithm with effort-reduction FLC technique is shown in Figure 3(a). In this algorithm, FLC is employed to eliminate the reliance on PI controller. The FLC technique employed performs by using voltage error *E(k)* and change of voltage error *CE(k)* with sample time *k* given in (4) and (8) respectively to approximate the required amplitude I_{dc}.

$$CE\,(k) = E(k) - E(k-1) \tag{8}$$

Generally, FLC operation involves four processes, starting with fuzzification, followed by fuzzy rule base and inference interpretation, and end with defuzzification. During fuzzification, the formulated numerical *E(k)* and *CE(k)* variables are converted into their corresponding linguistic representation, according to their respective fuzzy MFs. All input conditions will be processed by Mamdani-style fuzzy inference mechanism (Jain et al., 2002; Karuppanan &

Mahapatra, 2012; Suresh et al., 2012; Zainuri et al., 2016) to generate the most appropriate fuzzified I_{dc} output value according to the designed fuzzy rule base table which composes a collection of simple linguistic "If X and Y, Then Z" control rules. The generated fuzzified I_{dc} value is converted back to its corresponding numerical value via the defuzzification process. Most FLC techniques use the famous centroid of area (COA) defuzzification method (Suresh et al., 2012; Zainuri et al., 2016) as it provides a good average feature in determining the best output result. The normalized fuzzy MFs and rule base for proposed effort-reduction FLC technique are shown in Figure 3(b) and Table 1 respectively.

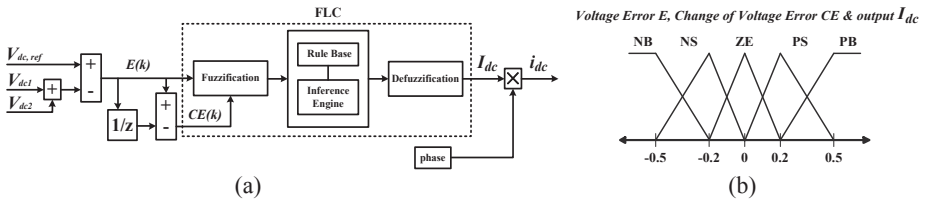


Figure 3. Proposed DC-link capacitor voltage regulation algorithm with effort-reduction FLC technique: (a) Control structure, and (b) Normalized fuzzy membership functions

Table 1
Fuzzy rule base for effort-reduction FLC technique

CEk	*E(k)*				
	NB	NS	ZE	PS	PB
NB	NB	NB	NB	NS	ZE
NS	NB	NB	NS	ZE	PS
ZE	NB	NS	ZE	PS	PB
PS	NS	ZE	PS	PB	PB
PB	ZE	PS	PB	PB	PB

The fuzzy sets were selected according to the degree of voltage error *E(k)* which may occur throughout the operation of SAPF. The selected fuzzy sets must possess certain sensitivity (level of fuzziness) which is sufficient enough to represent all the voltage error conditions. Low number of fuzzy sets may be insufficient to describe the characteristics of a signal. In contrast, large number of fuzzy sets provides much better results but high amount of fuzzy MFs and control rules are difficult to be developed.

In this study rather than relying on the complex FLC technique (7×7 fuzzy MFs with 49 control rules) which has widely been accepted as the best FLC design in the area of DC-link capacitor voltage regulation (Afghoul & Krim, 2012; Belaidi et al., 2012; Jain et al., 2002; Karuppanan & Mahapatra, 2010, 2012; Mikkili & Panda, 2012; Suresh et al., 2012), the effort-reduction FLC technique was developed by considering a reduced amount of fuzzy MFs and control rules: 5×5 fuzzy MFs with 25 control rules.

Our proposed effort-reduction FLC technique has also considered a combination of triangular and trapezoidal MFs. These types of fuzzy MFs are famous for their simple implementation features together with minimal computational efforts (Belaidi et al., 2012; Hoon et al., 2016a; Jain et al., 2002; Karuppanan & Mahapatra, 2012; Suresh et al., 2012). With utilization of the selected 5×5 fuzzy MFs in the proposed effort-reduction FLC technique, the overall DC-link voltage can constantly be maintained at desired value.

SIMULATION RESULTS

The three-phase three-level NPC inverter-based SAPF utilizing the proposed algorithm is simulated and evaluated in MATLAB-Simulink. The main specifications of the proposed SAPF are tabulated in Table 2. Simulation work is conducted under both steady and dynamic state conditions which involve two types of nonlinear loads. The first nonlinear load is constructed using a three-phase uncontrolled bridge rectifier feeding a 20 Ω resistor and 2200 μF capacitor connected in parallel (capacitive). The second nonlinear load is developed using similar rectifier feeding a series connected 50 Ω resistor and 50 mH inductor (inductive). Furthermore, to evaluate dynamic behaviour of the proposed algorithm, two dynamic state conditions can be created: capacitive to inductive load change and inductive to capacitive load change. However, due to limitation of pages, this work only considers dynamic state condition of capacitive to inductive load. Besides, evaluation under single dynamic state condition is good enough to evaluate the dynamic behaviour of the proposed algorithm. The conventional algorithm with PI technique was also tested for comparison purposes.

Table 2
Design specifications for SAPF

Parameter	Value
Voltage source	400 Vrms, 50 Hz
DC-link capacitor	3300 μF (each)
DC-link reference voltage	880 V
Limiting inductor	5 mH
Switching frequency	25 kHz

The simulation results of SAPF with effort-reduction FLC technique which include three-phase source voltage v_s, load current i_L , injection current i_{inj}, and source current i_s, for both nonlinear loads are shown in Figure 4. Meanwhile, THD values of source current i_s (phase A) before and after connecting the SAPF are summarized in Table 3. The findings clearly show that the THD values have been reduced to a level complying with the limit of 5 % set by IEEE Standard 519-2014 (IEEE, 2014). Moreover, SAPF with effort-reduction FLC technique has shown better harmonics mitigation performance as compared to PI technique. Furthermore, it can be observed that the mitigated source current i_s is working in phase with the source voltage v_s, thereby achieving almost unity power factor.

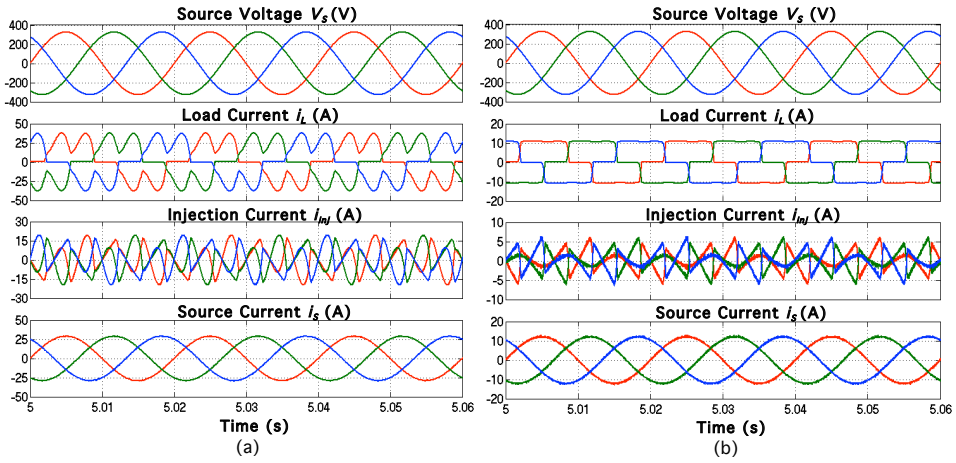


Figure 4. Simulation results of SAPF with effort-reduction FLC technique which include three-phase source voltage v_S, load current v_L, injection current i_{inj} and source current i_S for (a) capacitive, and (b) inductive loads

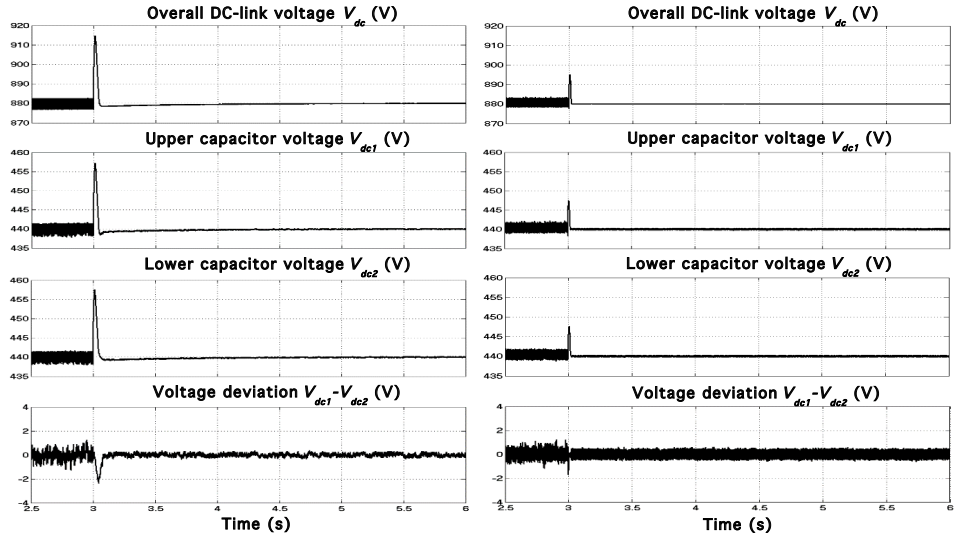


Figure 5. Simulation results of SAPF which include overall DC-link voltage V_{dc}, splitting DC-link capacitor voltages (V_{dc1} and V_{dc2}) and neutral-point voltage deviation (V_{dc1} - V_{dc2}) for dynamic state condition of capacitive to inductive load obtained using (a) conventional PI, and (b) proposed effort-reduction FLC techniques

Figure 5 shows the simulation results of SAPF which cover overall DC-link voltage V_{dc}, splitting DC-link capacitor voltages (V_{dc1} and V_{d2}), and neutral-point voltage deviation (V_{dc1} - V_{dc2})for dynamic state condition of capacitive to inductive load. Meanwhile, the performance of SAPF in term of overall DC-link voltage regulation is summarized in Table 3. From the findings, it is clear that the conventional algorithm with PI technique performs poorly with overshoot of 35 V, undershoot of 2 V, and response time of 1.50 s. In contrast, the proposed

algorithm with effort-reduction FLC technique performs outstandingly with overshoot of 15 V, undershoot of 0 V, and response time of 0.05 s. Therefore, in terms of overall DC-link voltage regulation, the proposed algorithm with effort-reduction FLC technique shows superior dynamic performance by achieving a response time of 30 times faster than the conventional algorithm with PI technique. In addition, it is clear that voltage across both splitting DC-link capacitors are successfully maintained as half of the overall DC-link voltage with minimum neutral-point voltage deviation and thus proving successful control of all DC voltages at their respective desired values.

Table 3
Overall performance comparison of both DC-link voltage regulation algorithms

DC-link voltage regulation algorithm	THD of Phase A Source Current i_s (%)		Dynamic Performance (Capacitive to Inductive)	
	Capacitive	Inductive	Overshoot/ Undershoot (V)	Response Time (s)
		Before Connecting SAPF		
N/A	43.03	27.43	N/A	N/A
		After Connecting SAPF		
PI technique	1.21	1.66	35 V (Overshoot) 2 V(Undershoot)	1.50 s
Effort-reduction FLC technique	1.19	1.63	15 V (Overshoot) 0 V(Undershoot)	0.05 s

CONCLUSION

This paper has successfully demonstrated a DC-link capacitor voltage regulation algorithm with effort-reduction FLC technique for three-phase three-level NPC inverter-based SAPF. The proposed algorithm with effort-reduction FLC technique provides an insight into developing a much simpler yet effective fuzzy-based algorithm for controlling the overall DC-link voltage of a typical inverter-based SAPF which was previously only achievable using complex fuzzy-based algorithm. The algorithm complexity is reduced by considering a reduced amount fuzzy MFs and control rules in controller design. As a result, the proposed algorithm is proven to provide successful control of overall DC-link voltage with superior dynamic performances. Low overshoot, no undershoot, and fast response time clearly show the advantages of proposed algorithm over the conventional algorithm especially in dealing with dynamic state condition.

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